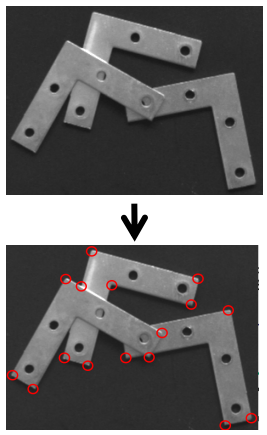
Multi-line buffer based pipeline architecture with Junction Connectivity and Inflection point selection for High Frame Rate and Ultra-Low Delay Contour-Based Corner Detection

查欣婧 池永研究室 修士課程修了

Background

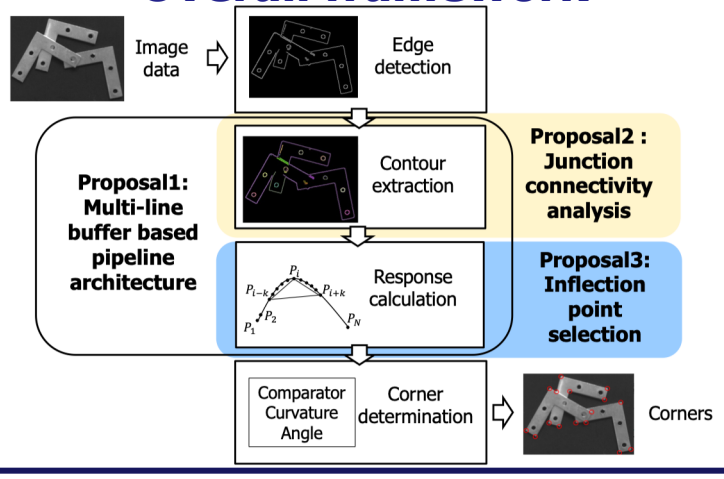
- Application
  - Workpiece positioning
  - Quality inspection
  - Motion tracking
  - …



- Target
  - High frame rate and ultra-low delay (1 msec/ frame) contour-based corner detection on FPGA
- Challenges
  - High accuracy and discrimination requirement
  - Ultra-low delay processing
  - …

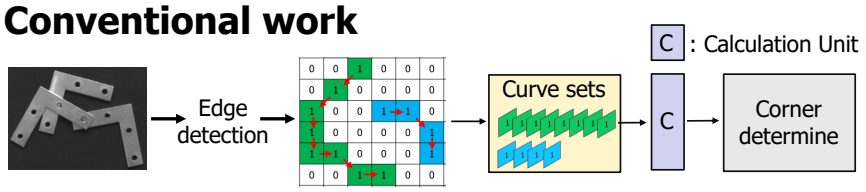
Proposed method

Overall framework

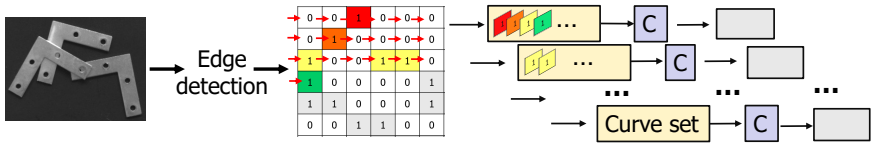


P1: Multi-line buffer based pipeline architecture

Conventional work

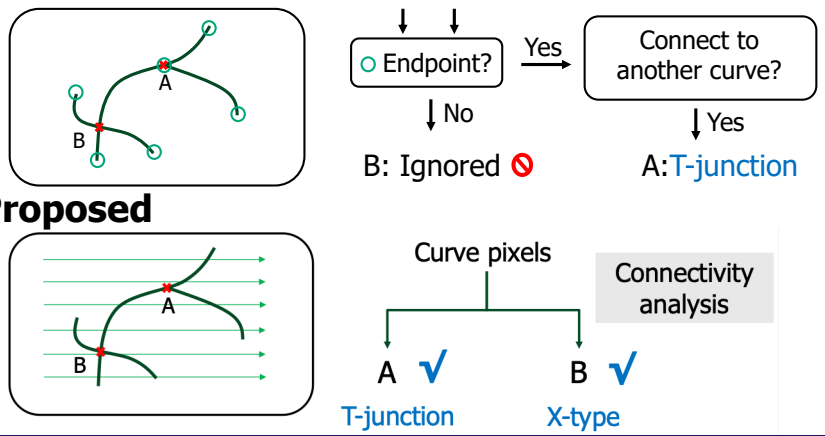


Proposed



P2: Junction connectivity analysis

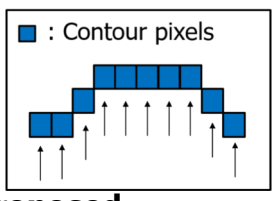
Conventional work



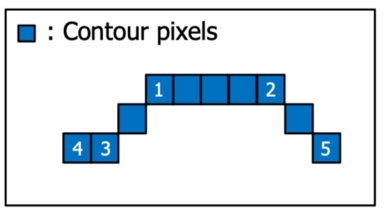
Proposed

P3: Inflection point selection with run-length coding

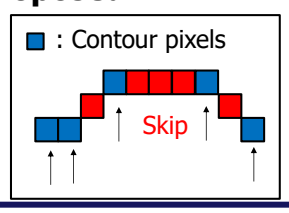
Conventional work



Run-length code



Proposed



Segment table	
1	(x_1, y_1)

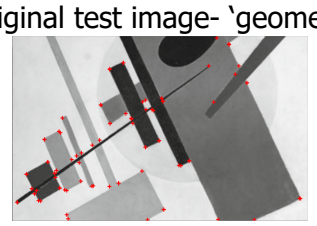
Links table		
1	Right 4	2
3	UpRight 2	1
4	Right 1	3
2	DownRight 2	5

Experiments Result

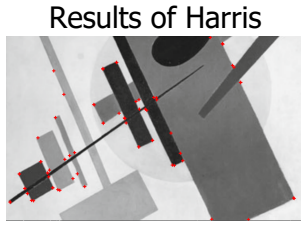
	Average Repeatability	Localization Error
Harris	0.5322398	0.7323982
CTAR	0.5832133	0.4373855
CTAR+P1	0.5714989	0.4284971
CTAR+P1+P2+P3	0.5714989	0.4284971

Original test image- 'geometric'

Results of Harris



Results of conventional CTAR



Results of CTAR + Proposal

Conclusion

- Hardware-oriented contour-based corner detection algorithm for high frame rate and ultra-low delay system

Graduate School of Information, Production and Systems
Waseda University